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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,534	11/26/2003	Dean A. Klein	MTIPAT.024DV4	1855

20995 7590 04/03/2007

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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/03/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/724,534	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-20,31,33,37-40 and 42-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-20, 31, 33, 37-40 and 42-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/17/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments with respect to claims 1-6, 8-20, 31, 33, 37-40 and 42-44 have been considered but are moot in view of the new ground(s) of rejection.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated January 17 2007 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 8-9, 11-16, 18-20, 31, 33, 37, 39-40 and 43-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Patent 5,948,100) in view of Simcoe (US Patent 6,000,008).

6. As per claims 1 and 12, Hsu teaches a method of performing a cache search operation within a digital processing system, searching a string of data for a match with a data string, the method comprising:

routing a series of assembly instructions to a processor (Fig. 8, ref. 100) having a first execution circuit (general execution circuit) (execution circuit 130 of Fig. 8) for executing arithmetic and logic instructions (Fig. 8 and col. 11, l. 40 to col. 12, l. 10), as the interrupt is received from a interrupt controller and is then forwarded to the execution unit (Fig. 8. ref. 130);

analyzing the series of assembly instructions (e.g. interrupt comprising the STA (program start address)) to detect a search instruction to perform a search operation, the search instruction comprising a data string (e.g. TAG) and a starting address (e.g. SET) for the search operation (Fig. 8-9, 14; col. 22, l. 31 to col. 23, l. 48 and col. 25, l.

61 to col. 26, l. 8), wherein the received interrupt inherently incur the search utilizing the search address (SA) = STA, wherein SA comprises the TAG data and the SET starting address (Fig. 9) and the search operation is perform by the branch target buffer (BTB 200 of Fig. 8 and col. 13, ll. 10-17);

routing the search instruction (e.g. SA = STA) undecoded to a data string manipulation circuit (Fig. 8, ref. 200), independent of the first execution circuit (general execution circuit) (execution circuit 130 of Fig. 8), capable of performing string manipulation instructions, without intervention by the first execution circuit (Fig. 9; Fig. 14; col. 22, l. 31 to col. 23, l. 52 and col. 25, l. 61 to col. 26, l. 8), wherein the received STA is directly transferred to BTB through the corresponding MUX (Fig. 14, ref. 425, 450) without the intervention of a decoder unit (Fig. 8, ref. 120) or the execution circuit (Fig, 8, ref. 130), therefore undecoded, and wherein the BTB receives and manipulates the STA in order to properly implementing the searching;

routing the starting address (SA comprising the SET starting address) for the search operation from the data string manipulation circuit to a cache memory array (Fig. 9, ref. 200, 210);

searching a cache line (cache block comprising 212, 214, 216, 218 of Fig. 9) in the cache memory for data that matches the data string (TAG) by comparing (utilizing comparators 244-1 to 244-4 and 226-1 to 226-4 of Fig. 9) the data string (TAG) with data stored in the cache memory array (Fig. 8-9, ref. 200), wherein said cache line comprises more bytes than the data string (col. 13, l. 41 to col. 14, l. 65), wherein the

cache block (cache line) comprises four blocks of data and the comparators attempts to match one of the four blocks to the data string; and

routing an address (predicted target address (TA) and predicted instruction address (PA)) of cached data matching the data string (TAG) to the data string manipulation circuit (fetcher 400 of Fig. 8) (Fig. 8).

Hsu does not teach the method of performing the cache search operation within the digital processing system, searching the string of data for the match with the data string, the method comprising:

comparing portions of the data string with consecutive portions of data stored in the cache memory array;

generating a match signal for each portion of the data stored in the cache memory that matches a respective compared portion of the data string; and

identify a plurality of match signals indicating sequential portions of the data stored in the cache memory that together match the data string.

Simcoe teaches a system and a method comprising:

a plurality of comparators (Fig. 2, ref. 24.1, 24.2) comparing portions (e.g. portions such as "SI," "MP," "SO," and "N -" of Fig. 7) of a sequential data (e.g. "SIMPSON") with consecutive portions of the data (e.g. data such as "SI," "MP," "SO," and "NX" of Fig. 7) stored in a cache memory array (Fig. 2, ref. 22.1, 22.2) (Abstract, col. 5, l. 57 to col. 6, l. 29 and col. 9, ll. 11-39);

generating a match signal for each corresponding matching portions by setting a match till now bit to "1" (Fig. 7); and

the combined matching signals indicate sequential portions of the data (e.g. "SI," "MP," "SO," and "NX" of Fig. 7) stored in the cache memory array combined matches the data string (e.g. "SIMPSON") (Abstract, col. 5, l. 57 to col. 6, l. 29 and col. 9, ll. 11-39).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Simcoe's matching of the sequential data with consecutive data stored in the cache memory array into Hsu's cache search operation. The resulting combination of the references further teaches the method of performing the cache search operation within the digital processing system, searching the string of data for the match with the data string, the method comprising:

the plurality of comparators comparing to match portions of the sequential data with the data stored in the cache memory array;

generating the match signal for each corresponding matching portions; and

the combined matching signals are utilized to identify that the sequential portions of the data stored in the cache memory array match the sequential data.

Therefore, it would have been obvious to combine Simcoe with Hsu for the benefit of searching for data with variable length in the cache memory (Simcoe, Abstract and col. 1, ll. 54-57).

7. As per claim 2, Hsu and Simcoe teach all the limitations of claim 1 as discussed above, where Hsu further teaches the method additionally comprising routing the data

string (e.g. SA comprising TAG) from the data string manipulation circuit (Hsu, Fig. 8, ref. 400) to the cache memory array (Hsu, Fig. 8-9, ref 200).

8. As per claims 3 and 13, Hsu and Simcoe teach all the limitations of claims 2 and 12 as discussed above, where Hsu further teaches the method additionally comprising aligning the data string with the data stored, by utilizing an offset (e.g. OFFSET) of the start address, in the cache memory array prior to said act of comparing (Hsu, Fig. 9 and col. 13, l. 42 to col. 14, l. 65), wherein the TAG is aligned utilizing OFFSET.

9. As per claims 4 and 16, Hsu and Simcoe teach all the limitations of claims 1 and 12 as discussed above, where both further teach the method comprising wherein said acts of identifying a plurality of matches signals (Simcoe, match till now logic 40 of Fig. 2) and routing an address of cached data is performed by a decoder (Hsu, priority decoders 232, 234 of Fig. 9) (Hsu, col. 14, l. 57 to col. 15, l. 57 and Simcoe, Abstract, col. 5, l. 57 to col. 6, l. 29 and col. 9, ll. 11-39).

10. As per claims 8 and 18, Hsu and Simcoe teach all the limitations of claims 1 and 12 as discussed above, where Hsu further teaches the method comprising wherein said act of comparing is performed by a plurality of comparators (Hsu, Fig. 9, ref. 244-1 to 244-4 and 226-1 to 226-4) (Hsu, col. 14, ll. 23-65).

11. As per claims 9 and 19, Hsu and Simcoe teach all the limitations of claims 1, 12, 31 and 40 as discussed above, where both further teach the method comprising wherein the number of plurality of comparators is equal to the number of bytes in a cache line of the cache memory array (Hsu, Fig. 9 and Simcoe Fig. 2, ref. 16.1, 16.2, 22.1, 22.2, 24.1, 24.2).

12. As per claims 11 and 20, Hsu and Simcoe teach all the limitations of claims 1 and 12 as discussed above, where Hsu further teaches the method comprising wherein said act of comparing is performed in one single clock cycle (Hsu, col. 2, ll. 1-21), as each stage of a pipeline requires one cycle to perform, such as fetching one instruction per cycle.

13. As per claim 14, Hsu and Simcoe teach all the limitations of claim 12 as discussed above, where Hsu further teaches the method comprising wherein the data string manipulation circuit comprises a bus interface unit (Hsu, control logic 435 of Fig. 14), wherein the control logic interfaces between the received interrupt comprising STA and what is actually sent to the BTB.

14. As per claim 15, Hsu and Simcoe teach all the limitations of claim 12 as discussed above, where Hsu further teaches the method comprising wherein the data string manipulation circuit comprises a memory controller (Hsu, control logic 435 of Fig. 14), wherein the control logic controls the MUX (Hsu, Fig. 14, ref. 425, 420), therefore

controlling what is inputted and stored into the memory comprising the SA register (Hsu, Fig. 14, ref. 410) and the FA register (Hsu, Fig. 14, ref. 405).

15. As per claim 31, Hsu teaches a processor comprising:

a data memory (Fig. 9, ref. 210) comprising a plurality of cache lines (Fig. 9, ref. 212, 214, 216, 218, wherein the plurality of cache blocks (cache line) comprises of four blocks of data), each cache line comprising a plurality of bytes of data (col. 13, ll. 41-65);

an instruction fetch circuit (fetcher 400 of Fig. 8);

a first instruction processing circuit (execution unit 130 of Fig. 8) coupled to the instruction fetch circuit (Fig. 8 ,ref. 400) and configured to perform arithmetic and logic instruction received from the instruction fetch circuit (col. 11, l. 40 to col. 12, l. 10);

a second instruction processing circuit (BTB 200 of Fig. 8-9) coupled to the instruction fetch circuit (Fig. 8, ref. 400) and configured to perform data string operation, the second instruction processing circuit being further configured to receive a data string (e.g. TAG) and an instruction to perform a search operation beginning at the starting address (e.g. SET) of the data memory, the second instruction processing circuit further comprising a plurality of inputs coupled to the data memory such that each input is coupled to receive one of the plurality of bytes of data of the cache line (col. 13, ll. 41-65 and col. 16, ll. 55-61), wherein upon receiving the search address (SA) the BTB inherently perform the search operation searching the plurality of cache blocks for data matching to the data string (col. 13, ll. 11-16 and col. 13, l. 42 to col. 14, l. 65).

Hsu does not teach the processor comprising:

each input is coupled to receive a different one of the plurality of data;

a plurality of comparators, each comparator coupled to a respective one of the plurality of inputs and configured to compare the byte of data of the cache line respective by the respective input with a portion of the data string, each comparator further configured to generate a match signal when the byte of data matches the compared portion of the data string, the plurality of comparators further comprises a plurality of outputs; and

a decoder circuit coupled to the plurality of outputs to receive match signals from the plurality of comparators configured to identify sequential portions of the cache line having data that, when combined, matched the data string.

Simcoe teaches a system and a method comprising:

a plurality of comparators (Fig. 2, ref. 24.1, 24.2) comparing a different one of the plurality of bytes of data (Fig. 2, ref. 16.1, 16.2, 22.1, 22.2), wherein the data are stored in the respective memories (Fig. 2, ref. 22.1, 22.2) (Fig. 7 and col. 5, ll. 57-64);

each comparator coupled to a respective one of the plurality of inputs and configured to compare the byte of data from the respective input with a portion of (e.g. portions such as "SI," "MP," "SO," and "N -" of Fig. 7) of a sequential data (e.g. "SIMPSON"), each comparator further configured to generate a match signal when the byte of data matches the compared portion of the sequential data, the plurality of comparators further comprises a plurality of outputs (Fig. 7; Abstract; col. 5, l. 57 to col. 6, l. 29 and col. 9, ll. 11-39); and

a match till now logic (Fig. 2, ref. 40) coupled to the plurality of outputs to receive match signals from the plurality of comparators configured to identify portion of the sequential data that, when combined, matched the data string (Fig. 7; Abstract; col. 5, l. 57 to col. 6, l. 29 and col. 9, ll. 11-39).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Simcoe's matching of the sequential data with data stored in the memory and match till now logic into Hsu's processor.

Therefore, it would have been obvious to combine Simcoe with Hsu for reason stated above in claims 1 and 12.

16. Claim 33 repeats the limitations of claims 9 and 19 and is therefore rejected accordingly.

17. As per claim 37, Hsu and Simcoe teach all the limitations of claim 31 as discussed above, where Hsu further teaches the processor comprising wherein the entire cache line is compared to the data string in one bus cycle (Hsu, Fig. 9 and col. 2, ll. 1-21), wherein the entire catch block (cache line) is compared in parallel and one instruction is fetched per cycle.

18. As per claim 39, Hsu and Simcoe teach all the limitations of claim 31 as discussed above, where Hsu further teaches the processor comprising wherein the second instruction processing circuit (Hsu, Fig. 9, ref 200) further comprises a memory

controller (Hsu, output selection circuit 270 of Fig. 9) (Hsu, col. 15, l. 59 to col. 16, l. 10), wherein the output selection circuit controls what is outputted from the BEB data RAM.

19. As per claim 40, Hsu teaches a cache memory circuit comprising:

a cache data memory means for holding at least one cache line comprising a plurality of bytes of data (Fig. 9, ref. 210, 212, 214, 216, 218 and col. 13, ll. 42-65), wherein the cache block (cache line) comprises of four blocks of data; and

means for searching (Fig. 8, ref. 200) the at least one cache line, wherein said means for searching is coupled to said cache data memory means and said data source means, and wherein said means for searching receives a starting address (e.g. SET) for a search operating of the at least one cache line (cache block) and aligns the data value with an offset (e.g. OFFSET) of the starting address to search the at least one cache line in one clock cycle for data that matches the data value (Fig. 8-9; col. 2, ll. 1-21 and col. 13, l. 42 to col. 14, l. 65), wherein each stage of a pipeline performs in one cycle, such as fetching one instruction per cycle;

means for performing arithmetic and logic operation (execution unit 130 of Fig. 8); and

means for receiving a series of instructions (fetcher 400 of Fig. 8), wherein said means for receiving is coupled to both said means for searching (Fig. 8, ref. 200) and said means for performing (Fig. 8, ref. 130), and means for receiving being further configured to forward a first instruction (e.g. interrupt comprising the STA (program start address)) associated with the searching operation to said means for searching and to

forward second instructions (e.g. interrupt forwarded to the decoder unit (Fig. 8, ref. 120) then to the execution unit (Fig. 8, ref. 130) associated with the arithmetic and logic operations to said means for performing (Fig. 8-9; Fig. 14; col. 22, l. 31 to col. 23, l. 52 and col. 25, l. 61 to col. 26, l. 8).

Hsu does not teach the cache memory circuit comprising:

searching multiple portions of the at least one cache line that matches compared portions of the data value; and

mean for detecting a string of matches between the multiple portions of the at least one cache line and the compared portions of the data value.

Simcoe teaches a system and a method comprising:

a plurality of comparators (Fig. 2, ref. 24.1, 24.2) able to search multiple portions of a memory (e.g. portions such as "SI," "MP," "SO," and "NX" of Fig. 7) for matches with a compared portions (e.g. portions such as "SI," "MP," "SO," and "N -" of Fig. 7) of a sequential data (e.g. "SIMPSON"), therefore implementing the detection of a string of matches between the multiple portions of the memory (Fig. 2, ref. 22.1, 22.2) and compared portion of the sequential data (Fig. 7; Abstract; col. 5, l. 57 to col. 6, l. 29 and col. 9, ll. 11-39).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Simcoe's matching of the sequential data with data stored in the memory into Hsu's cache memory circuit.

Therefore, it would have been obvious to combine Simcoe with Hsu for reason stated above in claims 1 and 12.

20. As per claim 43, Hsu and Simcoe teach all the limitations of claim 40 as discussed above, where Hsu further teaches the cache memory circuit comprising wherein the means for searching comprises a plurality of comparators (Hsu, Fig. 9, ref. 244-1 to 244-4 and 226-1 to 226-4).

21. Claim 44 repeats the limitations of claims 9 and 19 and is therefore rejected accordingly.

22. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Patent 5,948,100) and Simcoe (US Patent 6,000,008), and further in view of Sachs et al. (US Patent 4,860,192).

Hsu and Simcoe teach all the limitations of claims 1 and 12 as discussed above.

Hsu and Simcoe does not expressly teach the method comprising:

wherein the data string comprises a word;

wherein the data string comprises a doubleword; and

wherein the data string comprises a quadword.

Sachs teaches a cache system and method

wherein the cache memory stores a singleword per addressable line of cache storage (column 7, lines 1-5);

wherein the cache memory stores a doubleword per addressable line of cache storage (column 7, lines 1-5); and

wherein the cache memory stores a quadword per addressable line of cache storage (column 2, lines 26-34).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Sachs's singleword, doubleword and quadword into Hsu and Simcoe's data string.

Therefore, it would have been obvious to combine Sachs with Hsu and Simcoe for the benefit of enabling searching of words of multiple length, as Hsu and Simcoe's cache block comprises the maximum length of 16 bytes, enabling the storing up to a quadword.

23. Claims 10, 17 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Patent 5,948,100) and Simcoe (US Patent 6,000,008), and further in view of Tran et al. (US Patent 5,764,946).

Hsu and Simcoe teach all the limitations of claims 1, 12 and 40 as discussed above.

Hsu and Simcoe does not teach the method wherein said act of comparing is performed with a plurality of subtractors.

Tran teaches a system and a method for predicting an instruction fetch within an Instruction cache comprising:

wherein said act of fetching address is performed with a plurality of subtractors (col. 37, ll. 7-20 and col. 38, ll. 24-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Tran's subtractor into Hsu and Simcoe's act for comparing.

Therefore, it would have been obvious to combine Tran with Hsu and Simcoe for the benefit of proper calculation of the address (Tran, col. 38, ll. 24-33).

24. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Patent 5,948,100) and Simcoe (US Patent 6,000,008), and further in view of Hicks et al. (US Patent 6,085,291).

Hsu and Simcoe teach all the limitations of claim 31 as discussed above.

Hsu and Simcoe does not expressly teach the processor wherein the data memory comprises a Level 1 cache.

Hicks teaches a computer system comprising:

a processor (Fig. 1, ref. 106, 108, 110) comprising of an associated L1 cache (Fig. 1 ref. 112, 114, 116); and

a memory controller (Fig. 1, ref 104), wherein the memory controller is an off-chip memory controller, external to the processor.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hicks's L1 cache and memory controller into Hsu and Simcoe's processor's cache block.

Therefore, it would have been obvious to combine Hicks with Hsu and Simcoe because it is well known to one skilled in the art that cache memory of the processor

comprises L1 cache, because the processing speed of the L1 cache is comparable to the speed of the processor, therefore enable for the processor to obtain data stored in the L1 cache much faster, in comparison to a cache memory located exterior to the processor; and further more, it is well known to one skilled in the art for the memory controller to be associated with the processor, wherein the memory controller is utilized to control the system memory of the computer system.

V. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-6, 8-20, 31, 33, 37-40 and 42-44 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 27, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER